In The Specification

Please replace paragraph 003 with the following rewritten paragraph:

003 Planarization, for example, is ~~an~~ increasingly important in semiconductor manufacturing technology. As device sizes decrease, the importance of achieving high resolution features through photolithographic processes correspondingly increases thereby placing more severe restraints on the degree of planarity of a semiconductor wafer processing surface. Excessive degrees of process surface non-planarity will affect the quality of several semiconductor process<u>es</u> including, for example, in a photolithographic process, the positioning the image plane of the process surface within an increasingly limited depth of focus window to achieve high resolution semiconductor feature patterns.

Please replace paragraph 005 with the following rewritten paragraph:

005 In a typical process for forming conductive interconnections in a multi-layer semiconductor device, for example, a damascene process is used to form vias and trench lines for interconnecting different layers and areas of the multilayer device. Vias (e.g., V1, V2 etc. lines) are generally

used for vertically electrically interconnecting semiconductor device layers and trench lines (e.g., M1, M2, etc. lines) are used for electrically interconnecting semiconductor device areas within a layer. Vias and trench lines are typically formed as part of a damascene process. Although there are several different methods for forming damascene structures, one typical method generally involves patterning and etching a semiconductor feature, for example a via opening within an insulating dielectric layer to make contact with a conductive area within an underlying layer of the multilayer device. The via opening ~~(plug)~~ may then be filled with, for example, copper to form a via (plug) followed by a CMP step to remove excess metal deposited on the insulating dielectric layer surface and to planarize[d] the surface for a subsequent processing step. A second insulating dielectric layer is then deposited followed by patterning and etching the second insulating dielectric layer to form a trench opening situated over the via. The trench opening is then filled with a metal, for example, copper, to form trench lines (intra-layer horizontal metal interconnections). A second CMP step is then carried out similar to the first CMP step to remove excess metal and to planarize the process wafer surface in preparation for further processing.

Please replace paragraph 009 with the following rewritten paragraph:

009 During the CMP process, the top surface of the copper layer may be oxidized ~~and~~ to form[s] ~~copper oxide, for example~~ copper oxide (Cu_2O or CuO) or copper hydroxide ($Cu(OH)_2$). During the post-CMP cleaning process, typically involving rotary brush cleaning[,] in basic or neutral pH cleaning environments, the copper oxide or copper hydroxide does not dissolve and may be transferred to the brushes, thus loading the brushes. The contaminated (or loaded) brushes may then transfer the copper oxide or copper hydroxide contaminants to subsequently processed substrates during cleaning. This problem has been addressed by using slightly acidic cleaning solutions to aid in the dissolution of the copper oxide or copper hydroxide particles. Unfortunately, it has been found that the slightly acidic solution may accelerate the erosion of copper filled metal interconnect lines, although the mechanism for such erosion has not been entirely clear.

Please replace paragraph 0026 with the following rewritten paragraph:

0026 Although the method of the present invention is explained by reference to particular post CMP cleaning apparatus it will be appreciated that any type of semiconductor cleaning apparatus and cleaning method may advantageously be modified according to the present invention where the cleaning method or apparatus involves cleaning a copper containing substrate, for example a copper containing dielectric layer included in a semiconductor wafer, with a cleaning solution under acidic conditions where the copper containing substrate is subjected to incident light while in contact with the cleaning solution. By incident light is meant light ~~with a wavelength~~ having a wavelength of between about 300 nanometers and about 800 nanometers.